CLAIMS

What is claimed is:

1. A driver comprising:

a resistance network comprising a plurality of legs; and

a plurality of predriver circuits, each of the plurality of predriver circuits being associated with one of the plurality of legs of the resistance network, each predriver circuit receiving a first input to determine whether the predriver produces a signal and a second input to determine when to produce the signal.

2. The driver of claim 1, wherein the first input indicates whether the associated leg of the resistance network is active.

3. The driver of claim 2, wherein the second input to the predriver circuit indicates whether one of the plurality of legs of the resistance network is active.

4. The driver of claim 3, wherein the legs of the resistance network are in a certain order and wherein the second input for each predriver circuit is an input for a leg of the resistance network matched in a reversed order.

5. The driver of claim 3, wherein if a predriver circuit produces a signal:

the predriver circuit produces the signal after a first time interval if the second input to the predriver circuit indicates that the relevant leg is active; and

the predriver circuit produces after a second time interval if the second input to the predriver circuit indicates that the relevant leg is inactive.

6. The driver of claim 5, wherein slower conditions result in more active legs producing signals using a shorter time interval.

7. The driver of claim 5, wherein faster conditions result in more of the legs that are active producing signals using a longer time interval.

8. The driver of claim 1, wherein a predriver circuit comprises a passgate and a capacitor.

9. The driver of claim 8, wherein the second input to the predriver circuit is applied to the passgate, the second input determining whether the passgate opens or closes a path to the capacitor.

10. A method comprising:

receiving a first input and a second input for each of a plurality of signals,

wherein:

the first input for each of the plurality of signals indicates whether a resistance associated with the signal is active, the resistance comprising one leg of a resistance network, the resistance network comprising a plurality of legs, and

the second input indicates whether one leg of the plurality of legs of the resistance network is active;

determining whether to produce each signal based at least in part on the first input for the signal; and

determining when to produce each signal based at least in part on the second input for the signal.

11. The method of claim 10, wherein the legs of the resistance network are in a certain order and wherein the second input for each signal is matched in reverse order.

12. The method of claim 10, wherein determining whether to produce each signal comprises producing a signal if the first input for the signal indicates that the resistance associated with the signal is active.

13. The method of claim 10, wherein determining when to produce each signal comprises choosing to produce a signal after a first delay if the second input for the signal is active and choosing to produce the signal after a second delay if the second input for the signal is inactive.

14. The method of claim 13, wherein determining when to produce the signal comprises choosing to produce the signal after a shorter delay in slow conditions and choosing to produce the signal after a longer delay in fast conditions.

15. A device comprising:

an interface to a bus; and

an I/O driver circuit to drive signals on the bus, the I/O driver comprising:

a driver section; and

a predriver section comprising:

a resistance compensation network comprising a plurality of legs, and

a plurality of predriver circuits, each predriver circuit being associated with one of the plurality of legs, each predriver

circuit receiving a first input to determine if the predriver circuit produces a signal and a second input to determine the predriver circuit produces a signal..

16. The device of claim 15, wherein the first input to a predriver circuit indicates whether the associated leg of the resistance compensation network is active.

17. The device of claim 16, wherein the second input to a predriver circuit indicates whether one of the legs of the plurality of legs of the resistance network is active.

18. The device of claim 17, wherein the legs of the resistance network have a certain order and wherein the second input for each predriver circuit is an input for a leg of the resistance network matched in a reverse order.

19. The device of claim 17, wherein if a predriver circuit produces a signal:
the predriver circuit produces the signal after a first delay if the second input to the predriver circuit indicates that the relevant leg is active; and
the predriver circuit produces the signal after a second delay if the second input to the predriver circuit indicates that the relevant leg is inactive.

20. The device of claim 19, wherein if PVT (process, voltage, or temperature) conditions for the device result in slower operation, more of the active predriver circuits produce signals after a shorter delay.

21. The device of claim 20, wherein if PVT conditions for the device result in faster operation, more of the active predriver circuits produce signals after a longer delay.

22. The device of claim 15, wherein each predriver circuit comprises a passgate and a capacitor.

23. The device of claim 22, wherein the second input determines whether the passgate opens or closes a path to the capacitor.

24. A system comprising:

a processor;

a bus;

a driver to drive signals on the bus, the driver comprising:

a resistance network comprising a plurality of legs; and

a plurality of predriver circuits, each of the plurality of predriver circuits being associated with one of the plurality of legs of the resistance network, each predriver circuit receiving a first input to determine whether the predriver produces a signal and a second input to determine when to produce the signal.

25. The system of claim 24, wherein the first input to a predriver circuit indicates whether the associated leg of the resistance network is active.

26. The system of claim 25, wherein the second input to the predriver circuit indicates whether one of the plurality of legs of the resistance network is active.

27. The system of claim 26, wherein the legs of the resistance network are in a certain order and wherein the second input for each predriver circuit is an input for a leg of the resistance network matched in a reversed order.

28. The system of claim 26, wherein if a predriver circuit produces a signal:

the predriver circuit produces the signal after a first time interval if the second input to the predriver circuit indicates that the relevant leg is active; and

the predriver circuit produces after a second time interval if the second input to the predriver circuit indicates that the relevant leg is inactive.

29. The system of claim 24, wherein a predriver circuit comprises a passgate and a capacitor.